SMC-TR-98-15

AEROSPACE REPORT NO.
TR-93(3940)-12

Single-Word Multiple-Bit Upsets in Static Random Access Devices

15 January 1998

Prepared by

R. KOGA, S. D. PINKERTON, T. J. LIE, and K. B. CRAWFORD
Technology Operations

Prepared for

SPACE AND MISSILE SYSTEMS CENTER
AIR FORCE MATERIEL COMMAND
2430 E. El Segundo Boulevard
Los Angeles Air Force Base, CA 90245

Engineering and Technology Group

APPROVED FOR PUBLIC RELEASE;
DISTRIBUTION UNLIMITED

THE AEROSPACE CORPORATION
El Segundo, California

This report was submitted by The Aerospace Corporation, El Segundo, CA 90245-4691, under Contract No. F04701-93-C-0094 with the Space and Missile Systems Center, 2430 E. El Segundo Blvd., Suite 6037, Los Angeles AFB, CA 90245-4687. It was reviewed and approved for The Aerospace Corporation by A. B. Christensen, Principal Director, Space and Environment Technology Center. Maj. J. W. Cole was the project officer for the Mission-Oriented Investigation and Experimentation Program (MOIE) program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

J. W. Cole, Maj. USAF
SMC/AXES

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 January 1998	

4. TITLE AND SUBTITLE

Single-Word Multiple-Bit Upsets in Static Random Access Devices

5. FUNDING NUMBERS

F04701-93-C-0094

6. AUTHOR(S)

Koga, R.; Pinkerton, S.D.; Lie, T.J.; and Crawford, K.B.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

The Aerospace Corporation
Technology Operations
El Segundo, CA 90245-4691

8. PERFORMING ORGANIZATION REPORT NUMBER

TR-93(3940)-12

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Space and Missile Systems Center
Air Force Materiel Command
2430 E. El Segundo Blvd.
Los Angeles Air Force Base, CA 90245

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

SMC-TR-98-15

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

Space-borne electronics systems incorporating high-density static random access memory (SRAM) are vulnerable to single-word multiple-bit upsets (SMUs). We review here recent observations of SMU, present the results of a systematic investigation of the physical cell arrangements employed in several currently available SRAM device types, and discuss implications for the occurrence and mitigation of SMU.

14. SUBJECT TERMS

Heavy ion irradiation effects
Microcircuits in space
Multiple-bit upset
Radiation effects
Single event upset
Space-borne electronics
Static random access memory upset

15. NUMBER OF PAGES

9

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	

Single-word Multiple-bit Upsets in Static Random Access Devices

R. Koga, S.D. Pinkerton, T.J. Lie, and K.B. Crawford
The Aerospace Corporation
PO Box 92957, Los Angeles, CA 90009

Abstract Space-borne electronics systems incorporating high-density static random access memory (SRAM) are vulnerable to single-word multiple-bit upsets (SMUs). We review here recent observations of SMU, present the results of a systematic investigation of the physical cell arrangements employed in several currently available SRAM device types, and discuss implications for the occurrence and mitigation of SMU.

Introduction

Energetic ions and protons can cause single event upsets (SEUs) in static random access memory (SRAM) cells. In some cases multiple bits may be upset as the result of a single event. The possible occurrence of multiple-bit upsets in SRAMs exposed to the space radiation environment was first reported in 1983 [1]. Ground-based testing has confirmed that a single ion may alter more than one location in an SRAM device.

Multiple-bit upsets can be divided into two broad classes: the first (Type I) is due to an incident ion that is essentially parallel to the surface of the die intersecting the sensitive volumes of multiple memory cells, as shown in Fig. 1. Notice that the affected cells need not be adjacent on the die. Since the SRAM die is normally a rectangle with side length on the order of several millimeters, the range of the ions must be at least this great for such "lateral strikes" or "glancing collisions" to occur. This type of upset was observed at the Lawrence Berkeley Laboratory (LBL) Bevalac facility several years ago with two SRAM device types, 93L422 (256 x 4) and 27LS00 (256 x 1) [2,3], and more recently with the higher density IDT71256 (32K x 8) [4]. Double upsets have also been reported recently [5].

At other than near zero incidence angles (hence shorter ion ranges), only cells in close proximity can be upset, either because the track diameter spans the sensitive regions of multiple cells (e.g., high Z particle tracks), or by charge from the track entering the sensitive regions via diffusion [6]. The erroneous bits resulting from this type of upset (Type II) are observed at physically clustered memory cell locations. This mechanism has been shown to cause multiple-bit upsets in some devices, but not in others [7].

In general, multiple-bit upsets can be expected to involve more than a single logical memory word, i.e., the affected bits are likely to belong to different words. However, energetic particles may also upset more than one bit belonging to a single word, a phenomenon referred to as a "single-word multiple-bit upset" (SMU) [4]. This type of upset clearly depends on the physical arrangement and size of the memory cells. In particular, as cell sizes shrink and cell density increases, the prevalence of this type of upset can be expected to rise.

Since simple 1-bit error detection and correction (EDAC) algorithms cannot correct multiple erroneous bits within the same word, SMUs pose an even more substantial threat to system integrity than a simple count of the number of upset bits might indicate (i.e., whereas multiple bit errors within different words are easily corrected by 1-bit EDAC schemes, bits within the same word cannot be so corrected).

This paper presents the results of an investigation of the SMU vulnerability of a number of high density SRAM device types. The primary objectives of this study were to: (1) examine the extent of SMUs in SRAMs; (2) determine, where possible, design characteristics that predispose devices to this type of upset; and (3) investigate SMU mitigation techniques applicable to space-based electronic systems.

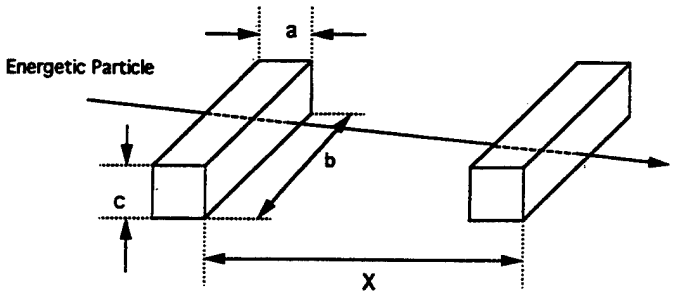

Fig. 1. SMU in physically separate cells
An energetic cosmic ray can upset two cells (separated by a distance x) in a single logical word. The larger the separation, the lower the probability of SMU.

Recent Observations of SMUs

A. Physically Separated Memory Cells (Type I SMUs)

As an example of the occurrence of SMUs in SRAMs, we shall consider a specific device type, the IDT71256 [4]. The IDT71256 is a 32K x 8 SRAM in which no logically adjacent cells (i.e., bits belonging to the same memory word) are physically adjacent on the die. A memory map for this device is shown in Fig. 2. The IDT71256 die measures approximately 6 x 8 mm, and is covered by a metal case whose outer dimensions are approximately 11 x 14 mm. The cells are arranged in a grid of 512 rows (along the y-axis) and 512 single-bit

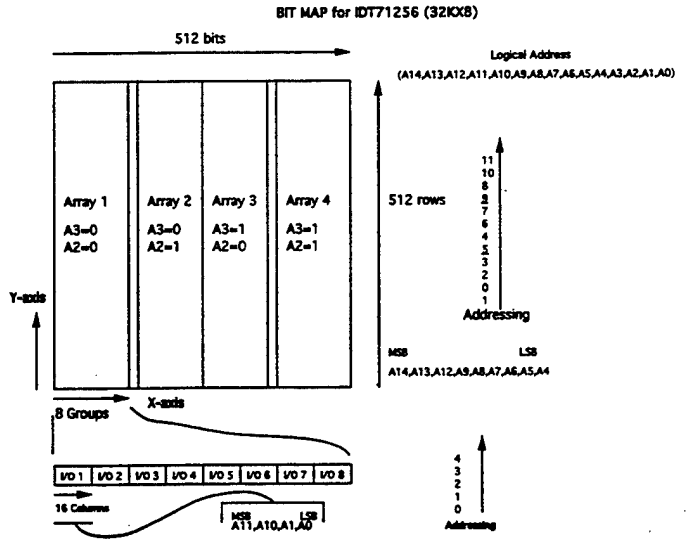

Fig. 2. Bit map for IDT71256 (32K x 8) SRAM

columns (along the x-axis), grouped into four arrays of 128 columns each (see Fig. 2). Each logical word consists of 8 bits from a single array. Logically adjacent bits are separated by 15 physical bits across the column.

To produce a multiple-bit upset in a single word an ion must traverse across the column (along the x-axis) and deposit sufficient charge at each of two logically adjacent bits, as shown in Fig. 1. Since logically adjacent bits are separated by a minimum of 15 physical memory cells, no fewer that 16 consecutive cells must be traversed. There is thus a small solid angle subtended at each bit site into which an energetic ion can enter and (possibly) cause an SMU. For the IDT device, this solid angle is $d\Omega = A/R^2 = 1.4 \times 10^{-3}$ ster, where A is the perpendicular area *bc* (see Fig. 1), and R is the distance spanning 16 cells along the x-axis. Ions traversing along the y-axis never encounter multiple bits belonging to the same logical word, and therefore cannot cause SMU in this device type.

The layout of a single IDT71256 memory cell – measuring about 9.7 x 11 x 3.5μ – is illustrated in Fig. 3. The SEU sensitive region is roughly "cigar shaped". A parallelpiped, *a* x *b* x *c*, can be used to approximate this shape. For the IDT71256, *a* is between 2 and 4 μm, *b* is between 5 and 8 μm, and *c* is about 3.5 μm (*a* is along the x-axis and *b* is along the y-axis).

A test of the SMU vulnerability of the IDT71256 was conducted at the LBL Bevalac facility using silicon (282 MeV/nucleon) and iron (410 MeV/nucleon) ions with linear energy transfer (LET) values of 0.6 and 1.7 MeV/(mg/cm^2), respectively. The range of these ions in silicon is about 3 cm. The test device was mounted on a special test board that could be rotated via remote control during irradiation. During exposure, all SRAM cell locations were interrogated by the test control computer, starting with logical address 0000 (hex) and extending to the maximum address. Upsets were documented, tallied, and corrected as soon as detected by the computer. This process was repeated until a sufficient number of errors had been collected for the particular incidence angle. The beam angle was then changed and this process repeated.

As expected from the elongated shape of the cells, there were substantial directional differences in the threshold LETs: ~3 MeV/(mg/cm^2) along the x-axis and less than 1.7 MeV/(mg/cm^2) along the y-axis [4]. However, SMUs were observed only along the x-axis, due to the lay-out of the cells on the die.

Figure 4 shows the total number of multiple bit errors observed along the y-axis as the beam angle varied from the horizontal. Although these errors were not SMUs (as noted above, SMUs cannot arise in the y direction), they were generated by the same mechanism as is responsible for SMUs along the x-axis. As shown in this figure, the number of errors falls off as the disparity from the horizontal is increased (in this case, the horizontal is *defined* as the angle that maximizes the occurrence of this type of error).

We calculated an expected SMU rate of 1×10^{-4} words/(dev-day) in geosynchronous orbit [4], using an extension of the CREME code (called MULTSEU) that combines information on device geometry with the measured SEU vulnerability and expected radiation environment to predict the Type I SMU rate in space.

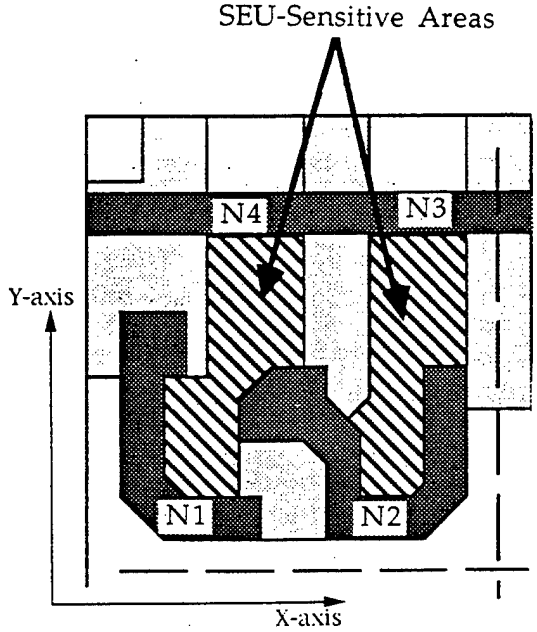

Fig. 3. Schematic of IDT71256 memory cell
Field oxide regions are shown in light gray; poly gate regions are shown in dark gray.

B. Physically Adjacent Memory Cells (Type II SMUs)

In the Hitachi HM628128 128K x 1 SRAM, a logical word (byte) consists of two sets of 4 bits that are physically adjacent along the x-axis. (The two sets are

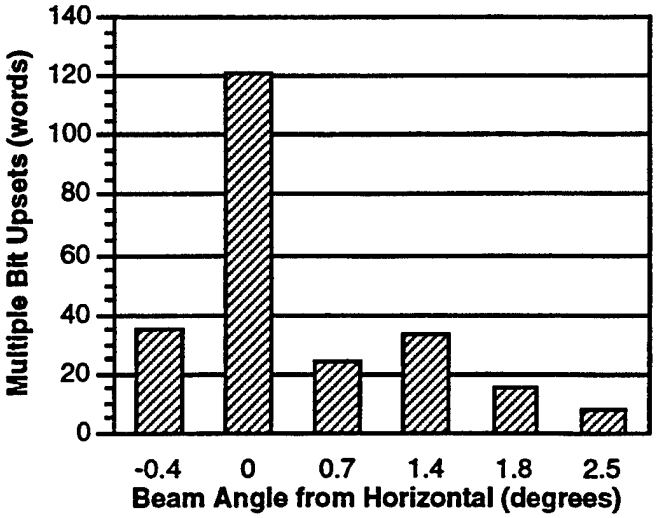

Fig. 4. Multiple bit errors along y-axis
Data from 410 MeV iron beam oriented parallel to y-axis of the IDT71256 die.

separated by 32 bits along the x-axis.) It is therefore not surprising that this device type is highly susceptible to SMU caused by heavy ions impinging normal to the surface of the die [7]. (The die for MSM8128 in Ref. [7] is identical to that for HM628128.)

In contrast, the physical layout of the Micron Technology MT5C1008 ensures that logically adjacent bits are separated by at least 16 physically adjacent cells. No SMUs were observed for this device type when it was irradiated with heavy ions normal to the chip surface, despite the frequent occurrence of physically adjacent cells being upset by the same ion [7]. This device might be susceptible to Type I SMUs under certain circumstances, however (as is the similarly configured IDT71256).

Additional SMU Related Concerns

A. Word-line Upsets

An additional class of non-random errors in SRAMs, "word-line upsets" has recently been proposed by McDonald et al. [8], who investigated their occurrence in IDT71682 (4K x 4) and IDT71256 SRAMs. For these upsets it is suspected that a single ion strike at the control node of the word-line can cause bit errors at multiple address locations connected by the word-line, by creating a spurious write condition. McDonald et al. observed patterns of errors consistent with the word-line upset hypothesis. However, their data also admit alternative explanations since they do not report the time of occurrence of the individual bit-upsets. To substantiate the word-line hypothesis would require evidence that the multiple errors they observed in single words were temporally coincident (or nearly so), as would result from a word-line upset.

In an effort to observe word-line errors, we tested IDT7164 (8K x 8) and IDT71256 SRAMs at the LBL 88-inch cyclotron facility using N, Ne, Ar, and Cu ions. (Most of the tests were conducted using Ne ions to minimize latchup.)

Our testing procedure was as follows: first the device was "filled" with a known bit pattern. Then, while the device was exposed to the ion beam, the memory locations were continuously interrogated, errors detected/corrected and documented. (Memory locations were exercised in order of ascending addresses, beginning at logical address 0, up to the maximum address, then back to 0, and repeat). Since the read cycle time was about 2.5 μsec and the write time was also fast, we did not lose an appreciable amount of the beam time (with respect to the total exposure time) during the correct/document periods. After a sufficient number of data points had been gathered, we closed the beam shutter, thereby ending the "run".

On each run it took 3 to 4 minutes to accumulate about 20 errors. The typical error rate was therefore about 0.1 per second. Because each error was time-tagged and stored in computer memory, we were able to identify the bit errors caused by a single incident ion.

Although we were able to duplicate the bit error pattern reported in [8], it appeared to have been caused by an accumulation of single-bit errors, rather than by a hit in the word-line control circuit, as indicated by an examination of the time-tags associated with the individual errors. However, the source of this pattern remains a mystery; it may be due to some unknown architecture-dependent mechanism.

B. Periodic Removal of SEUs

The natural accumulation over time of single-bit SEUs in a die (or possibly a larger memory system) increases the probability that multiple bits in the same logical word will be in error. Periodic "scrubbing" or "washing" of the memory is therefore required to eliminate these SEUs. Scrubbing is normally accomplished by reading, correcting (via an EDAC), and writing back to the memory. If a single-bit EDAC scheme is utilized, SMUs cannot be corrected by this method; hence, scrubbing must be performed frequently to lessen the accumulation of SMUs. We suspect that most SEU-vulnerable SRAMs employed in space are periodically subjected to some form of scrubbing.

C. "Stuck" Bits

Some SRAM device types are prone to a form of damage characterized by the presence of a semi-permanently stored bit pattern. In some cases multiple bits within a single logical word are "stuck" in this fashion.

Table 1. Summary of Device Types in SMU Study

Device ID	Mfr.	Organization	Cell Separation†
HM628512	Hitachi	512K x 8	1 (8 bit group)
HM628128	Hitachi	128K x 8	1 (4 bit group)
IDT71024	IDT	128K x 8	8
MT5C1008	Micron	128K x 8	16
MC6226	Motorola	128K x 8	16
EDH8832	EDI	32K x 8	16
IDT71256	IDT	32K x 8	16
CDM62256	GE	32K x 8	16
HM62256	Hitachi	32K x 8	16

† Minimum number of bits along the x-axis an ion must traverse to cause SMU

Table 2. Expected SMU Rate at Geosynchronous Orbit

Device ID	Mfr.	SMU Rate*
HM628512	Hitachi	6×10^{-1}
HM628128	Hitachi	3×10^{-1}
IDT71024	IDT	8×10^{-4}
MC6226	Motorola	4×10^{-4}
MT5C1008	Micron	2×10^{-4}
EDH8832	EDI	1×10^{-4}
IDT71256	IDT	1×10^{-4}
CDM62256	GE	1×10^{-4}
HM62256	Hitachi	6×10^{-5}

* Upset words/device-day predicted using MULTSEU.

This form of damage has been observed during exposure to heavy ions since the mid 1980's, but was not reported in the literature until 1991 [7]. Shortly thereafter, Dufour et al. [9] completed an in-depth study of this phenomenon, which they called "single hard errors (SHE)".

The presence of "stuck" bits creates a very real problem that can be expected to affect some of the SRAM types utilized in space systems. Fortunately, many "stuck" bits anneal spontaneously.

D. SMU Vulnerabilities of Selected SRAMs

Table 1 lists, in increasing order of SMU vulnerability, some of the device types that have been considered in the present SMU study. Because these devices do not differ substantially in their bitwise SEU vulnerability, the SMU susceptibility is largely a function of the spacing between logically adjacent bits. Not surprisingly, the 512K x 8 and 128K x 8 Hitachi devices, in which groups of 8 and 4 bits per logical word, respectively, are physically adjacent, show the greatest susceptibility to SMU. The 32K x 8 devices and the Micron Technology and Motorola 128K x 8 parts, in contrast, are much less vulnerable to SMU because logically adjacent bits are widely separated.

Before these devices can be incorporated into space system designs, it is important to assess their vulnerability to SMUs in the space radiation environment. Table 2 lists the expected Type I SMU rates for several SRAM device types at geosynchronous orbit, calculated using the MULTSEU code described above.

SMU Mitigation

Because most non-radhard high density SRAMs have a rather low LET threshold for random SEUs, as shown in Figs. 5-8, one might expect the SMU susceptibility to be correspondingly high. However, the SEU vulnerability of the individual cells is only one factor that influences the SMU probability. The SMU rate also critically depends on the architecture of the die (or memory system). For example, as reported above, the arrangement/spacing of the memory cells in the MT5C1008 significantly attenuates its Type II SMU vulnerability. Similarly, although the Motorola MC6226 and the Hitachi HM628128 memory cells have comparable SEU sensitivities (compare Figs. 5 and 7), their susceptibilities to Type I SMUs differ by several orders of magnitude, as shown in Table 2.

Thus, careful design at the die or device level can be quite effective at lessening the threat of SMU. Further mitigation can be achieved at higher system levels. Such concerns are especially relevant to the design of space systems. Among the design related considerations for the mitigation of SMU at the memory system level are the following:

(1) SRAMs organized "by one" (e.g., 256K x 1) could be used to reduce the probability of SMU by increasing (by several orders of magnitude) the distance between bits belonging to the same logical word.

(2) Shielding could also be employed to reduce the threat of Type I SMUs. For example, in order to cause an SMU in the IDT71256, an energetic ion must traverse within a narrow solid angle on the order of 1×10^{-3} ster. Hence, the material needed to attenuate a 1 GeV/n Fe ion is 0.3 g/device (formed to the solid angle). Although the amount of shielding material required is small, proper alignment may be difficult in practice.

(3) Since it may be impossible to abolish SMUs completely, sophisticated multiple-bit EDAC algorithms could be employed to correct the erroneous bits arising from SMUs. (Simple EDAC algorithms enable two bit-errors within a word to be detected, but only a single bit to be corrected, and therefore cannot be used for SMU mitigation.) Unfortunately, more complicated EDAC schemes are likely to raise costs and reduce the speed of operation of the memory system.

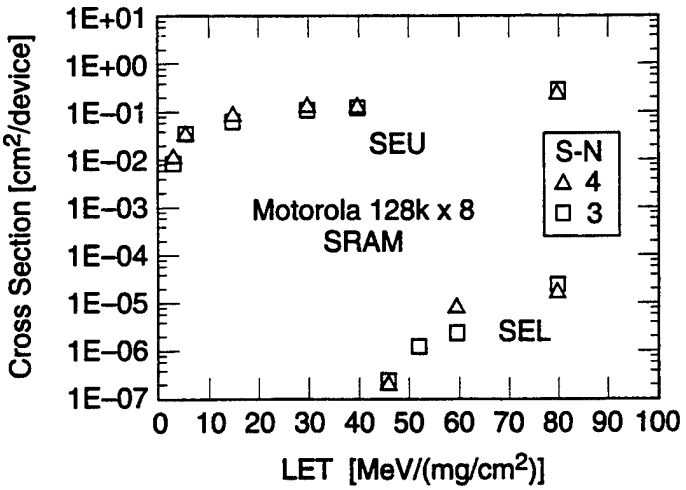

Fig. 5. SEU and SEL cross-sections for Motorola MC6226 128K x 8 SRAM (SEL = Single event latchup)

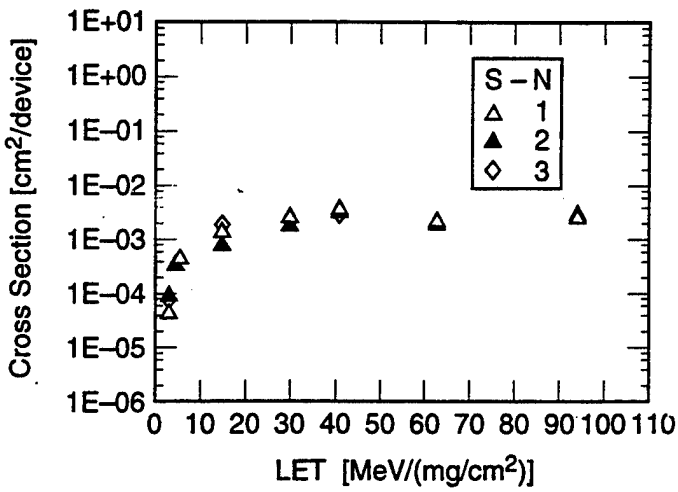

Fig. 6. SEU cross-section for Micron Technology MT5C1008 128K x 8 SRAM (No latchup was observed)

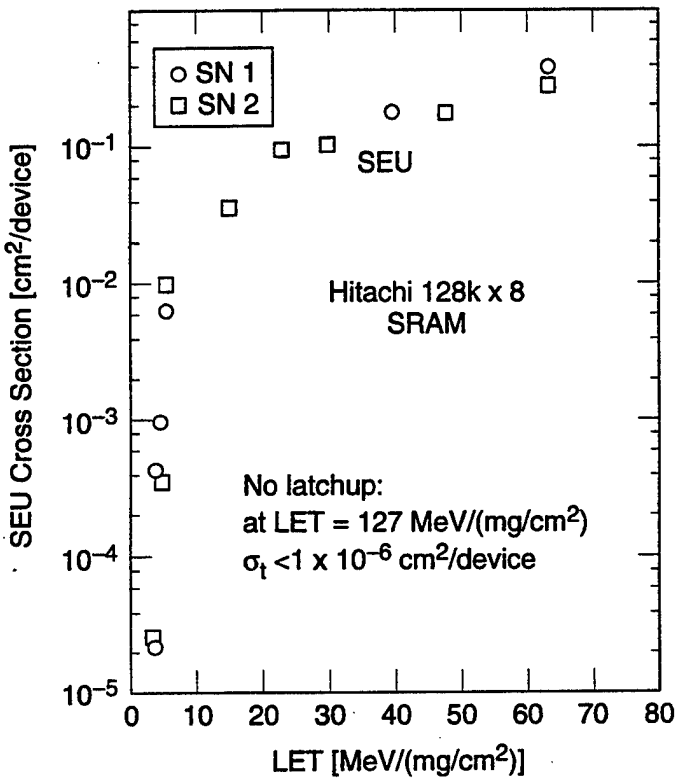

Fig. 7. SEU and SEL cross-sections for Hitachi HM628128 128K x 8 SRAM

Conclusion

As magnetic tape recorders are replaced by gigabit capacity solid state recorders fashioned from high density SRAMs, threat of SMU becomes an important consideration in the design of memory systems to be incorporated into space applications, particularly since conventional 1-bit EDAC algorithms cannot correct SMUs. This threat can be ameliorated through proper design at both the device and system levels, shielding, and the incorporation of multiple-bit EDAC schemes into critical circuits.

The results reported above suggest that a non-negligible SMU rate can be expected for most high density SRAM types when exposed to the space radiation environment. However, the range of SMU rates is also very large, suggesting that the careful selection of device types should be emphasized during the design phase. Furthermore, susceptibility to SEU is not necessarily a reliable indicator of SMU vulnerability. A more important determinant, in many cases, is the architecture of the device, especially the physical separation between logically adjacent cells. It is therefore inappropriate to consider SEU studies a proxy for SMU investigations.

We are currently in the process of extending our SMU study to include additional high density memory devices, such as 16-megabit SRAMs.

Acknowledgments

We would like to express our gratitude to the Aerospace technical staff for their assistance in all phases of the testing procedure. We also would like to thank the staffs of the LBL Bevalac and 88-inch cyclotron facilities for beam delivery.

References

1. Blake, J.B. and R. Mandel, "On-orbit Observation of Single Event Upset in Harris HM-6508 1K RAMs," IEEE Transactions on Nuclear Science, NS-33, 1616-1619, 1986.
2. Criswell, T.L., P.R. Measel, and K.L. Walin, "Single Event Upset Testing with Relativistic Heavy Ions," IEEE Transactions on Nuclear Science, NS-31, 1559-1561, 1984.

3. Criswell, T.L., D.L. Oberg, J.L. Wert, P.R. Measel, and W.E. Wilson, "Measurement of SEU Thresholds and Cross Sections at Fixed Incident Angles," IEEE Transactions on Nuclear Science, NS-34, 1316-1321, 1987.
4 Koga, R., K.B. Crawford, P.B. Grant, W.A. Kolasinski, D.L. Leung, T.J. Lie, D.C. Mayer, S.D. Pinkerton, and T.K. Tsubota, "Single Ion Induced Multiple-bit Upset in IDT 256K SRAMs," Proceedings of the Second European Conference on Radiation and Its Effects on Devices and Systems (RADECS '93), submitted, 1993.
5. Smith, E.C., and M. Shoga, "Double Upsets from Glancing Collisions: A Simple Model Verified with Flight Data," IEEE Transactions on Nuclear Science, 39, 1859-1864, 1992.
6. Martin, R.C., N.M. Ghoniem, Y. Song, J.S. Cable, "The Size Effect of Ion Charge Tracks on Single Event Multiple-bit Upset," IEEE Transactions on Nuclear Science, NS-34, 1305-1309, 1987.
7. Koga, R., W.R. Crain, K.B. Crawford, D.D. Lau, S.D. Pinkerton, B.K. Yi, and R. Chitty, "On the Suitability of Non-hardened High Density SRAM's for Space Applications," IEEE Transactions on Nuclear Science, 38, 1507-1513, 1991.
8. McDonald, P.T., W.J. Stapor, A.B. Campbell, and L.W. Massengill, "Non-Random Single Event Upset Trends," IEEE Transactions on Nuclear Science, 36, 2324-2329, 1989.
9. Dufour, C., P. Garnier, T. Carrière, J. Beaucour, R. Ecoffet, and M. Labrunée, "Heavy Ion Induced Single Hard Errors on Submicronic Memories," IEEE Transactions on Nuclear Science, 39, 1693-1697, 1992.

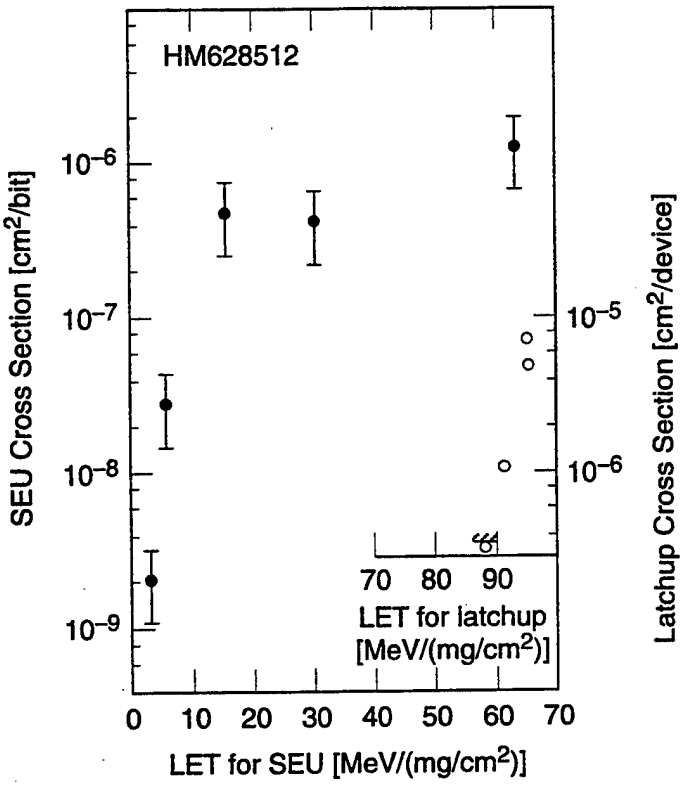

Fig. 8. SEU and SEL cross-sections for Hitachi HM628512 512K x 8 SRAM

TECHNOLOGY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security programs, specializing in advanced military space systems. The Corporation's Technology Operations supports the effective and timely development and operation of national security systems through scientific research and the application of advanced technology. Vital to the success of the Corporation is the technical staff's wide-ranging expertise and its ability to stay abreast of new technological developments and program support issues associated with rapidly evolving space systems. Contributing capabilities are provided by these individual Technology Centers:

Electronics Technology Center: Microelectronics, VLSI reliability, failure analysis, solid-state device physics, compound semiconductors, radiation effects, infrared and CCD detector devices, Micro-Electro-Mechanical Systems (MEMS), and data storage and display technologies; lasers and electro-optics, solid state laser design, micro-optics, optical communications, and fiber optic sensors; atomic frequency standards, applied laser spectroscopy, laser chemistry, atmospheric propagation and beam control, LIDAR/LADAR remote sensing; solar cell and array testing and evaluation, battery electrochemistry, battery testing and evaluation.

Mechanics and Materials Technology Center: Evaluation and characterization of new materials: metals, alloys, ceramics, polymers and composites; development and analysis of advanced materials processing and deposition techniques; nondestructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; analysis and evaluation of materials at cryogenic and elevated temperatures; launch vehicle fluid mechanics, heat transfer and flight dynamics; aerothermodynamics; chemical and electric propulsion; environmental chemistry; combustion processes; spacecraft structural mechanics, space environment effects on materials, hardening and vulnerability assessment; contamination, thermal and structural control; lubrication and surface phenomena; microengineering technology and microinstrument development.

Space and Environment Technology Center: Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing, hyperspectral imagery; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; component testing, space instrumentation; environmental monitoring, trace detection; atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, and sensor out-of-field-of-view rejection.